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A Boost Type Nine-Level Switched Capacitor Inverter

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Abstract–A new boost type multilevel inverter using switched capacitor structure is proposed. The main feature of the proposed inverter is boosting and multilevel output with small number of components. Due to the passive voltage balancing of each capacitor maintains a constant voltage without additional control. In this paper, the operation principle, the modulation method, the voltage/current stress on switches and the determination of capacitances, the simulation results with MATLAB/SIMULINK R2015a, the experimental results, and the 2 kW simulation are shown. The simulation and the experiments were conducted under resistive load and inductive load conditions. And the load variation was conducted in the experiment. Under both resistive load and inductive load conditions, the obtained waveforms by simulation and experiment agreed well with the theory. In the load variation experiment, the obtained waveforms were not distorted and the capacitor voltages maintained constant.

Index Terms–Multilevel inverter, switched capacitor, multicarrier PWM.

I. Introduction

Dependence on power generation with fossil fuels has been reviewed due to depletion problems and environmental impact. As an alternative energy, a large number of researchers have been focused on renewable energy, such as photovoltaic and wind [1]. In renewable energy systems, power electronic circuits play an important role to supply power stably and efficiently [2], [3].

Multilevel inverter is one of the circuit configurations aiming for high power conversion efficiency by reduction of switching losses, less total harmonic distortion (THD), good electromagnetic compatibility, and low voltage stresses [4], [5]. There are three types of basic multilevel inverters: cascaded H-bridge (CHB) [6]-[8], neutral point clamped (NPC) [9]-[11], and flying capacitor (FC) [12]-[14] inverters. However, by increasing the number of levels of these inverters, they require a huge number of switching devices, their drivers, and voltage sources, and may have a problem of capacitor voltage unbalance. Active neutral point clamped (ANPC) inverter [15]-[17] suppresses the number of components, however the capacitor voltage unbalance remains. Two solutions against the problem are using some auxiliary circuits or choosing redundant operation states.

When some types of multilevel inverters are applied to a grid-connected system, boost circuits [18]-[20] are required at the preceding stage depending on the system because the output voltages of the fuel cells and photovoltaic modules are relatively low compared with the grid voltage. When the boost circuits include inductors or transformers, the circuits become large and heavy [21]-[23]. On the other hand, in the case of charge pump, no boost inductor is needed.

The charge pump is a circuit which outputs a voltage larger or smaller than the input voltage by using switched capacitors [24]-[26]. The fundamental operation of the circuit is charging capacitors by connecting them with an input voltage source in parallel and discharging them connected in series or vice versa.

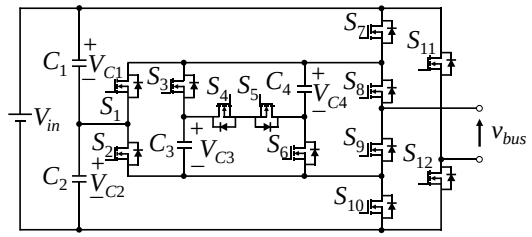

Fig. 1 Hybrid nine-level inverter with series/parallel conversion.

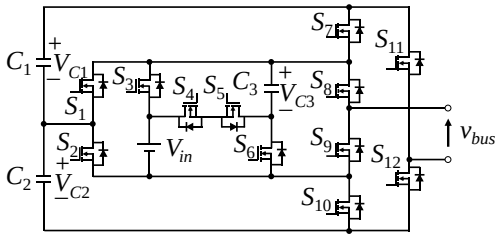

Fig. 2 Boost type nine-level switched capacitor inverter.

When the charge pump is used to boost the voltage, the output voltage becomes sum of the input voltage and the capacitor voltages. Inverters using this feature are called switched capacitor (SC) inverters [27]-[29]. These inverters make it easy to increase the number of levels and keep the capacitor voltages at a desired value owing to the principle of charge pump. Furthermore, it is possible to output a voltage larger than the input voltage without using inductors or transformers.

An SC inverter proposed in [30] outputs nine steps with fewer components than conventional nine-level inverters. However, it operates as a step-down inverter. This paper proposes a step-up SC inverter which outputs four times amplitude of the input voltage and nine steps of bus voltage waveform based on the SC inverter of [30] with the same circuit topology.

In the next section, the circuit description, operation principle, control strategy, the voltage/current stress on switches, the determination of capacitance, and comparison with conventional circuits are presented. After that, in Sections III and IV, simulation results with MATLAB/SIMULINK R2015a and experimental results are shown. In Section V, a 2 kW simulation is conducted.

II. Proposed Circuit

A. Circuit Description

Fig. 1 shows a hybrid nine-level inverter with series/parallel conversion (H9ISPC) proposed in [30], which is composed of an input voltage source V_{in}, four capacitors C_1 - C_4, and twelve switches S_1 - S_{12}. The H9ISPC outputs nine-level bus-voltage with fewer components than conventional nine-level inverters and each capacitor voltage is naturally maintained. This circuit is designed for step-down operation. Since the capacitors maintain their voltage constant, these capacitors can be regarded as constant voltage sources. By arranging the position of the capacitors and the voltage sources in the H9ISPC, it is possible to make it a step-up inverter. One idea is to replace the capacitor C_1 or C_2 with a floating power source and the other is to replace the capacitor C_3 or C_4 with a floating power source. The first one realizes double boosting and the second one does quadruple boosting. This paper focuses on the quadruple boosting circuit. A circuit

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topology of the proposed inverter is shown in Fig. 2. In order to increase the number of levels and step-up ratio, it is conceivable to increase the switched capacitor cells as in [27]. Fig. 3(a) shows the extended circuit topology for 9+4x (x = 1, 2,...) levels. x is the number of additional switched capacitor cells, which are composed of four switches and a capacitor. The amplitude of the bus voltage is (4+2x)V_{in}. In the circuit configuration shown in Fig. 3(b), the number of levels is 9+8y (y = 1, 2,...), where y is the number of additional pairs of switched capacitor cells. Each of them consists of three switches and a capacitor. The amplitude of the bus voltage is (4+4y)V_{in}. Another possible way to extend the number of levels is to connect the proposed inverter like CHB types.

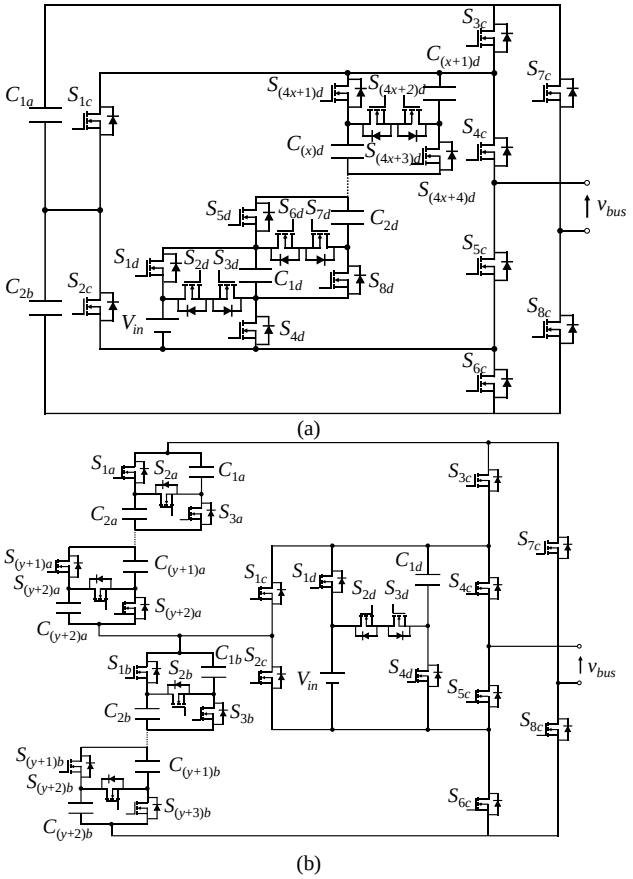

Fig. 3 Proposed circuit when extending the number of levels.

B. States of Circuit

In this paper, we focus on the circuit topology shown in Fig. 2. This inverter has nine switching states. In this section, five states of the nine 'States A to E' corresponding to the positive half cycle of the bus voltage are described, which are shown in Fig. 4. To make the concept more accessible, the capacitor voltages are assumed to be constant at $V_{C1} = V_{C2} = 2V_{in}$ and $V_{C3} = V_{in}$.

State A: When the switches S_2, S_4, S_5, S_7, S_8, and S_{12} are in ON state as shown in Fig. 4 (a), the bus voltage v_{bus} is

$$v_{bus} = V_{C2} + V_{in} + V_{C3} = 4V_{in}. \quad (1)$$

In this state, the series-connection of the capacitor C_3 and the voltage source V_{in} is connected in parallel with the capacitor C_1. Therefore, the capacitor voltage V_{C1} equals the sum of the input voltage V_{in} and the capacitor voltage V_{C3}. The capacitor C_1 is charged and the capacitors C_2 and C_3 are discharged during the term.

$$V_{C1} = V_{in} + V_{C3} = 2V_{in}. \quad (2)$$

State B: When the switches S_2, S_3, S_6, S_8, and S_{12} are in ON state as shown in Fig. 4 (b), the bus voltage v_{bus} is

$$v_{bus} = V_{C2} + V_{in} = 3V_{in}. \quad (3)$$

In this state, the capacitor C_3 is connected in parallel with the voltage source V_{in}. Therefore, the capacitor voltage V_{C3} equals the input voltage V_{in}. During the State B, the capacitor C_3 is charged while the capacitor C_2 is discharged.

State C: When the switches S_1, S_4, S_5, S_8, S_{10}, and S_{12} are in ON state as shown in Fig. 4 (c), the bus voltage v_{bus} is

$$v_{bus} = V_{in} + V_{C3} = 2V_{in}. \quad (4)$$

In this state, the series-connection of the capacitor C_3 and the voltage source V_{in} is connected in parallel with the capacitor C_2. Therefore, the capacitor voltage V_{C2} equals the sum of the input voltage V_{in} and the capacitor voltage V_{C3}.

$$V_{C2} = V_{in} + V_{C3} = 2V_{in}. \quad (5)$$

The capacitor C_2 is charged and the capacitor C_3 is discharged.

State D: When the switches S_1, S_4, S_5, S_8, S_{10}, and S_{12} are in ON state as shown in Fig. 4 (d), the bus voltage v_{bus} is

$$v_{bus} = V_{C2} - V_{C3} = V_{in}. \quad (6)$$

In this state, the capacitor C_3 is connected in parallel with the voltage source V_{in}. Therefore, the capacitor C_3 is charged and the voltage V_{C3} equals the input voltage V_{in}. The capacitor C_2 is discharged.

State E: When the switches S_9, S_{10}, and S_{12} are in ON state as shown in Fig. 4 (e). The bus voltage v_{bus} is

$$v_{bus} = 0. \quad (7)$$

Since the proposed inverter has a symmetric operation, it can be considered for the other four states in negative half cycle as well. Table I summarizes all the states for the proposed inverter where the bus voltage v_{bus} is obtained based on the ideal circuit model that is no parasitic components, no line impedance, and ideal switches.

C. Operation Principle and Control Strategy

There are a lot of control strategies for multilevel inverters [31]-[34]. In this paper, the level-shift (LS) PWM [34] is employed. When LS-PWM is applied to a single-phase z-level inverter ($z \geq 3$, odd number), z-1 carrier waveforms and one sinusoidal signal waveform are used. Since the proposed inverter outputs nine levels, the switching pattern is determined by comparing eight triangle carriers e_k (k = 1, 2,... 8) with a sinusoidal signal waveform e_s. Each carrier has the same amplitude of 0.5 and the same frequency f_s with the same phase angle. Their levels are shifted as shown in Fig. 5. The sinusoidal signal waveform $e_s = A\sin 2\pi f_{ref} t$ shares with these carriers on the same time axis. A is an amplitude $|A| < 4$ and f_{ref} is a frequency of the signal waveform.

As shown in Fig. 5. The modulation process is split into eight sectors according to the relationship between e_s and e_k. In each sector, two states alternately appear. In Sector 1, the signal waveform e_s is compared with the carrier waveform e_4. States D and E alternately appear and form the PWM bus voltage v_{bus} between V_{in} and 0. In Sector 2, the signal waveform e_s is compared with the carrier waveform e_3, thus States C and D alternately appear and the bus voltage v_{bus} takes $V_{in} + V_{C3} = 2V_{in}$ or V_{in}. In Sector 3, the signal waveform e_s is compared with the carrier waveform e_2. States B and C alternately appear and the bus voltage v_{bus} shuttles between

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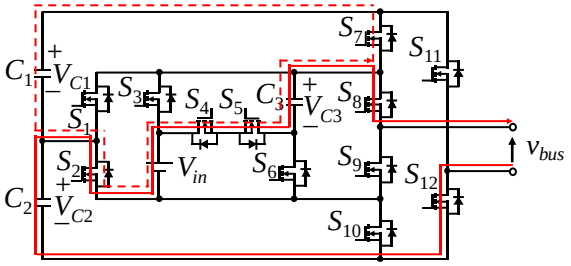
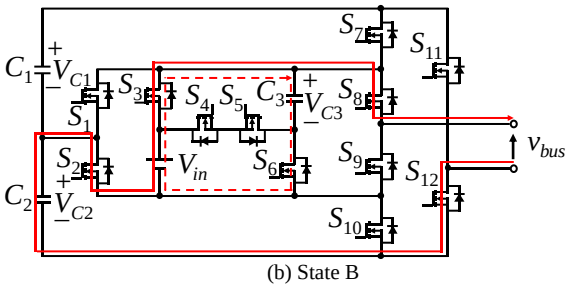
TABLE I SWITCHING STATES FOR THE PROPOSED INVERTER

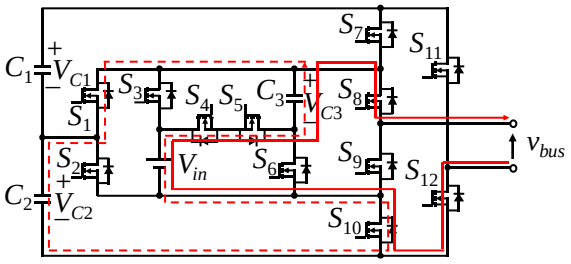
Relationship between e_s and e_k	State	Ideal bus voltage v_{bus}	On-state switches	Capacitor C_1	Capacitor C_2	Capacitor C_3
$e_s > e_1$	A	$4V_{in}$	S_2, S_4, S_5, S_7, S_8, S_{12}	Charge	Discharge	Discharge
$e_1 \geq e_s > e_2$	B	$3V_{in}$	S_2, S_3, S_6, S_8, S_{12}	None	Discharge	Charge
$e_2 \geq e_s > e_3$	C	$2V_{in}$	S_1, S_4, S_5, S_8, S_{10}, S_{12}	None	Charge	Discharge
$e_3 \geq e_s > e_4$	D	V_{in}	S_1, S_3, S_6, S_9, S_{12}	None	Discharge	Charge
$e_4 \geq e_s > e_5$	E	0	S_9, S_{10}, S_{12}	None	None	None
$e_5 \geq e_s > e_6$	-	$-V_{in}$	S_2, S_3, S_6, S_8, S_{11}	Discharge	None	Charge
$e_6 \geq e_s > e_7$	-	$-2V_{in}$	S_2, S_4, S_5, S_7, S_9, S_{11}	Charge	None	Discharge
$e_7 \geq e_s > e_8$	-	$-3V_{in}$	S_1, S_3, S_6, S_9, S_{11}	Discharge	None	Charge
$e_s \leq e_8$	-	$-4V_{in}$	S_1, S_4, S_5, S_9, S_{10}, S_{11}	Discharge	Charge	Discharge



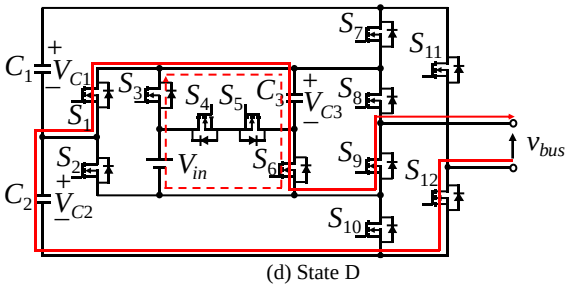
(a) State A



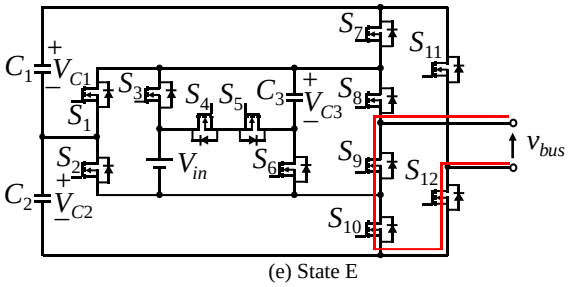
(b) State B



(c) State C



(d) State D



(e) State E

Fig. 4 Current flows in the proposed inverter.

$V_{in} + V_{C3} = 2V_{in}$ and $V_{in} + V_{C2} = 3V_{in}$. In Sector 4, States A and B provide the bus voltage v_{bus} between $4V_{in}$ and $V_{in} + V_{C2} = 3V_{in}$.

Since the proposed inverter has a symmetric operation, it can be considered for the negative half cycle as well.

D. VOLTAGE/CURRENT STRESSES ON SWITCHES AND DETERMINATION OF CAPACITANCES

The SC type inverter has a voltage ripple in each capacitor. A large voltage ripple causes deterioration of power conversion efficiency and THD. Therefore, appropriate design is required for the capacitors. According to [27] and [31], each capacitance is calculated from their voltage ripple. Assuming that the power factor of the output load $\cos\phi = 1$, the longest discharging period of the capacitor C_2 is the period in which the states of A and B are alternately repeated. In other words, it is the term between t_a and t_b as shown in Fig. 6. When the switching frequency f_s is sufficiently higher than the signal waveform frequency f_{ref}, the time t_a and t_b can be expressed as

$$t_a = \frac{\sin^{-1}(3E_c / M)}{2\pi f_{ref}}, \tag{8}$$

$$t_b = \frac{\pi - \sin^{-1}(3E_c / M)}{2\pi f_{ref}}. \tag{9}$$

From the relationship between the output current i_{out} and the discharging term of the capacitor C_2, the maximum discharging amount Q_2 of the capacitor C_2 is calculated by

$$Q_2 = \int_{t_a}^{t_b} I_{bus} \sin(2\pi f_{ref} t - \phi), \tag{10}$$

where I_{bus} is the amplitude of the output current i_{out} and ϕ is the phase difference between the output voltage v_{out} and the output current i_{out}. When an allowance of the voltage ripple ΔV_{C2} of the capacitor C_2 is given, the capacitance C_2 needs to be

$$C_2 \geq \frac{Q_2}{\Delta V_{C2}}. \tag{11}$$

Because of the symmetrical operation, the capacitance C_1 is similarly determined.

The voltage ripple of capacitor C_3 occurs when the capacitor voltage V_{C2} is smaller than $V_{in} + V_{C3}$ and the proposed inverter is in the state of Fig. 4(c). Fig. 7 shows the discharging period of capacitor C_3. At this time, the current of capacitor i_{C3} is the sum of the currents following to the load and the capacitor C_2. Therefore, the current of capacitor i_{C3} is

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$$i_{C3}(t) = \frac{V_{in} + v_{C3}(t) - v_{C2}(t)}{r_{in} + r_{C2} + r_{C3} + 4r_{DS}} + I_{bus}\sin(2\pi f_{ref} t - \phi), \quad (12)$$

where r_{C2} and r_{C3} are the equivalent series resistance (ESR) of the capacitors C_2 and C_3. r_{DS} is on resistance of the switch. The discharging term of the capacitor C_3 is from t_{2m-1} to t_{2m} (m = 1, 2,...n). By using (12), the discharging amount between t_{2m-1} and t_{2m} is calculated by

$$\Delta Q_3 = \int_{t_{2m-1}}^{t_{2m}} i_{C3}(t)dt \,. \quad (13)$$

The total discharging amount Q_3 is given as

$$Q_3 = \sum_{m=1}^{n} \Delta Q_3 \,. \quad (14)$$

In the term from t_1 to t_{2m}, the capacitor C_3 repeats charging and discharging. In the worst case, no charging term is given. The voltage reduction reaches Q_3/C_3. By determining the voltage ripple of the capacitor C_3 as ΔV_{C3}, the capacitor C_3 needs to satisfy

$$C_3 \geq \frac{Q_3}{\Delta V_{C3}} \,. \quad (15)$$

Table II shows voltage and current stresses of the switches. The maximum current of the capacitor C_3 is expressed as I_{C3m} and the maximum current of the output current is expressed as I_{busm}. The outermost switches S_{11} and S_{12} have the highest voltage stress and the switches existing in the path of charging capacitor C_1 or C_2 has the largest current stress. Regarding the current stress, it can be reduced by decreasing the voltage ripple of each capacitor according to the equation (12).

E. Comparison with Conventional Circuits

A comparison between the proposed inverter and the conventional single phase nine-level inverters is shown in Table III. From Table III, the proposed inverter has the smallest number of elements. Furthermore, the proposed inverter has the amplitude of the output voltage four times the input voltage; thus, no boost circuit is required in the preceding stage. In addition, no auxiliary circuit is required to keep capacitor voltages. Although FC type is considered as active balancing, passive balancing is realized in [35] with a 7-level FC inverter. A drawback of the proposed inverter is an isolated dc power source.

III. Simulation Results

In this section, two simulations were conducted using MATLAB/SIMULINK R2015a based on the experimental conditions. One was with a resistive load Z_1 which is a resistor R_1 and the output power was 50.5 W. The other one was with an inductive load Z_2 which consisted of an inductor L and a resister R_2 connected in series and the apparent power was 51.4 VA. Fig. 8 shows a simulation model of the proposed inverter and Table IV shows the parameters in the simulation. The modulation index A was adjusted to 3.64 to output 50 V as the rms value. The on-resistances r_{DS1} - r_{DS10} and the drain-source capacitances C_{DS1} - C_{DS10} of the MOSFETs S_1 - S_{10} were determined based on the datasheet of IRFB4410. The on resistances r_{DS11} and r_{DS12}, and the drain-source capacitances C_{DS11} and C_{DS12} of the MOSFETs S_{11} and S_{12} were based on the datasheet of IRFP4321. Each capacitance was designed to have a voltage ripple less than 10%. voltage v_{bus} had nine steps and the maximum voltage was about four times the input

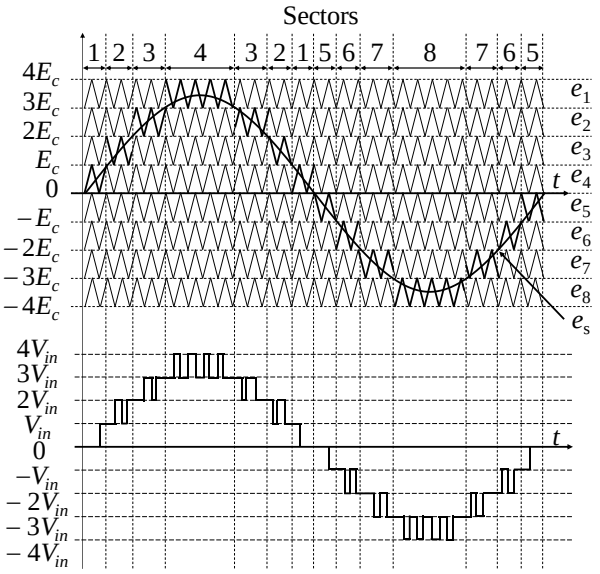

Fig. 5 Level Shift PWM for the proposed inverter.

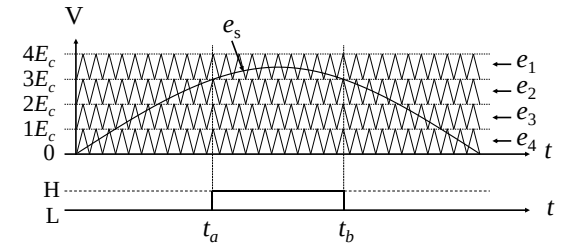

Fig. 6 Discharge period of capacitor C_2 using LS-PWM.

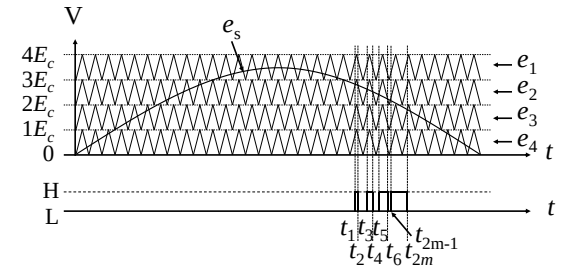

Fig. 7 Discharge period of capacitor C_3 using LS-PWM.

TABLE II Voltage and Current Stresses of The Switches

Switches	Maximum Voltage	Maximum Current
S_1, S_2, S_7, S_{10}	$2V_{in}$	I_{C3m}
S_8, S_9	$2V_{in}$	I_{busm}
S_3, S_4, S_5, S_6	V_{in}	I_{C3m}
S_{11}, S_{12}	$4V_{in}$	I_{busm}

voltage. The output voltage v_{out} was 50.2 V, while the theoretical value of the output voltage v_{out} is

$$\frac{AV_{in}}{\sqrt{2}} = 51.5 \quad V \,, \quad (14)$$

which was different from the simulation result. The voltage ripple of the capacitors and on-resistances of the MOSFETs could be the reason. The output current was in phase with the output voltage and the amplitude was 1.44 A. Fig. 9(b) shows the capacitor voltages V_{C2} and V_{C3}. V_{C1} is not described because it is symmetrical with V_{C2}. The ripple voltages of the capacitors were less than 10% as designed.

Fig. 10 shows the observed waveforms with the inductive load Z_2 in the simulation. From Fig. 10(a) and (b), they were similar to the waveforms shown in Fig. 9(a) and (b).

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TABLE III COMPARISON OF SINGLE PHASE NINE-LEVEL INVERTERS

		CHB [6]	NPC [9]	FC [12]	ANPC [15]	SCISPC [27]	Proposed circuit
DC power sources	Floating	3	0	0	1	1	1
	Grounded	1	1	1	1	0	0
Switches		16	16	16	12	13	12
Diodes		0	14	0	0	0	0
Capacitors		0	8	9	3	3	3
Boost circuit		Need	Need	Need	Need	No need	No need
Capacitor balance		None	active	active	passive	passive	passive

TABLE IV PARAMETERS OF THE PROPOSED INVERTER

Parameters	Value	Model number
Input voltage V_{in}	20.0 V (r_{in} : 50 mΩ)	KIKUSUI PWR400L
Modulation index A	3.64	-
Output load Z_1	R_1: 49.5 Ω	-
Output load Z_2	R_2: 42.2 Ω L: 78.9 mH	-
MOSFETs S_1 ~ S_{10}	r_{DS1} ~ r_{DS10} : 10.0 mΩ C_{DS1} ~ C_{DS10} : 107 pF	IRFB4410 (100V/96A)
MOSFETs S_{11}, S_{12}	r_{DS11}, r_{DS12} : 15.5 mΩ C_{DS11}, C_{DS12} : 307 pF	IRFP4321 (150V/78A)
Capacitor C_1	4.33 mF (r_{C1} : 11.2 mΩ)	2AUTES102M0×4
Capacitor C_2	4.32 mF (r_{C2} : 10.9 mΩ)	2AUTES102M0×4
Capacitor C_3	2.19 mF (r_{C3} : 20.3 mΩ)	2AUTES102M0×2
Capacitor C_S	1.12 mF (r_{CS} : 40.3 mΩ)	2AUTES102M0×1
Filter inductor L_f	1.05 mH (r_{Lf} : 58.8 mΩ)	PC95PQ32/20Z
Filter Capacitor C_f	487 μF (r_{Cf} : 201 mΩ)	2EMMSSDC474KE
Switching frequency f_s	20.0 kHz	-
Frequency of the reference waveform f_{ref}	50.0 Hz	-
Time step	1.00×10^{-8} s	-

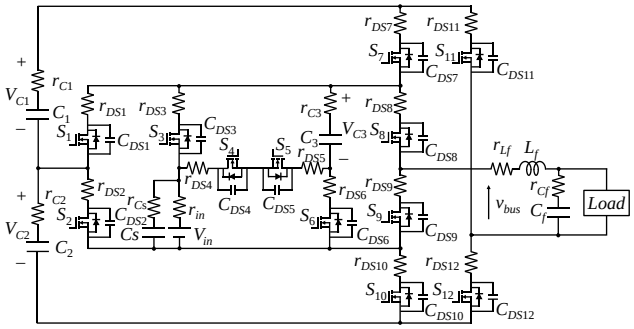
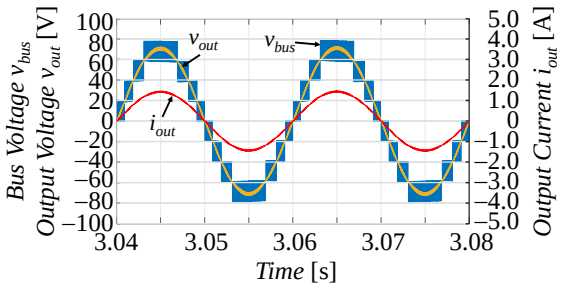
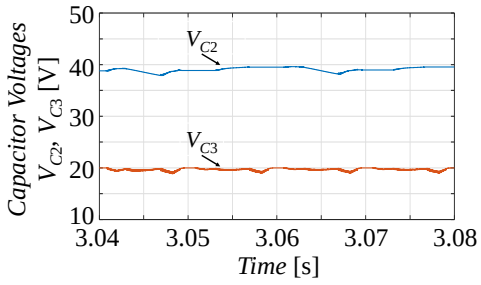


Fig. 8 Simulation model of proposed inverter.



(a)



(b)

Fig. 9 Observed waveforms with the resistive load Z_1 in the simulation,(a) bus voltage v_{bus}, output voltage v_{out}, output current i_{out}, (b) capacitor voltages V_{C2} and V_{C3}.

In Fig. 10(a), there was a phase difference between the output voltage and the output current. The phase difference corresponded to the power factor of the inductive load Z_2 with $\cos\phi = 0.862$.

The spectra observed in the simulation are shown in Fig. 11. Fig. 11(a) and (b) are the spectra of bus voltage v_{bus} and output current i_{out} with the resistive load Z_1. Fig. 11(c) and (d) are those with the inductive load Z_2. The vertical axis presents magnitudes normalized with the fundamental component.

Under the resistive load condition, as shown in the Fig. 11(a) and (b), THD of the bus voltage and the output current were respectively 16.6 % and 1.78 %. Under the inductive load condition, as shown in Fig. 11(c) and (d), THD of the bus voltage and the output current were respectively 16.5 % and 0.24 %. The harmonic components of the output current is reduced as compared with Fig. 11(b). This is because the inductive load plays a role of a filter. From Fig. 11, it was confirmed that the proposed inverter operated accurately even in inductive load condition.

IV EXPERIMENTAL RESULTS

In order to verify operation of the proposed inverter, a reduced scale prototype circuit was built and tested. Values of the passive components were measured with an impedance meter HIOKI IM3536 and shown in Table IV, which were common to the simulation parameters. As a control circuit, an FPGA Cyclone EP1C3T100C8 was used. The power conversion efficiency and the power factor was measured with YOKOGAWA PZ4000 power analyzer. Waveforms were observed with Tektronix TPS2014 oscilloscope. A picture of the prototype circuit is shown in Fig. 12.

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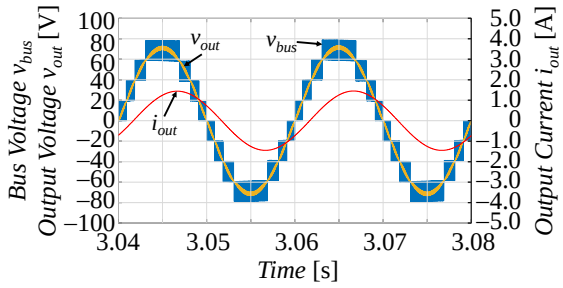
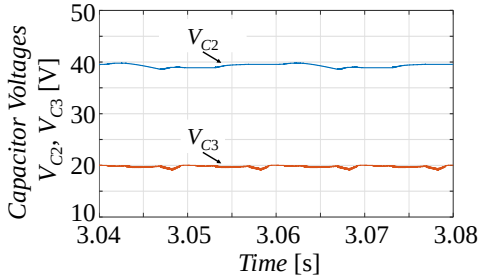
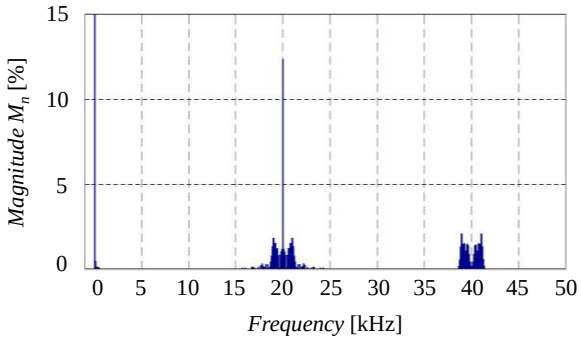


(a)

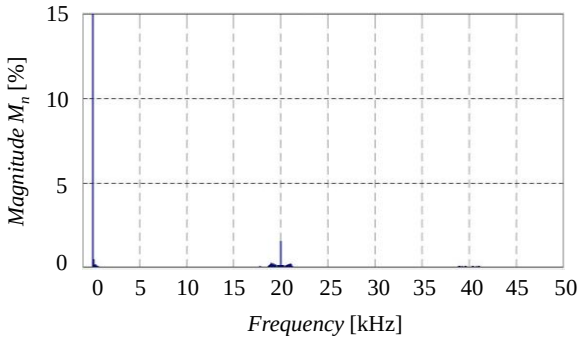


(b)

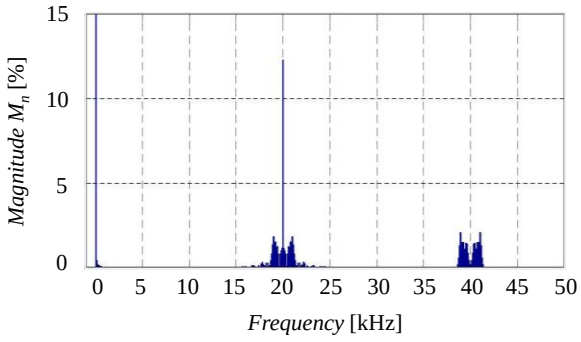
Fig. 10 Observed waveforms with the inductive load Z_2 in the simulation,(a) bus voltage v_{bus}, output voltage v_{out}, output current i_{out}, (b) capacitor voltages V_{C2} and V_{C3}.



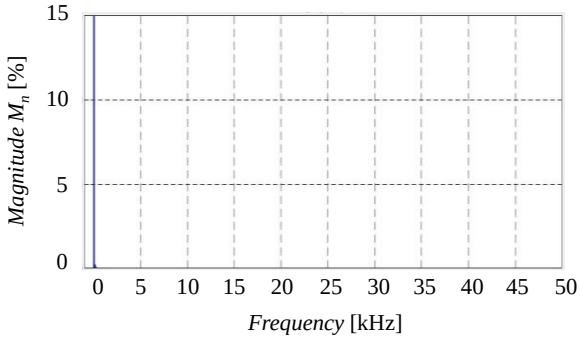
(a)



(b)



(c)



(d)

Fig. 11 The spectrums observed in the simulation, (a) bus voltage v_{bus} with Z_1, (b) output current i_{out} with Z_1, (c) bus voltage v_{bus} with Z_2, (d) output current i_{out} with Z_2.

The circuit experiment was conducted under three conditions. 1) the inverter was loaded with a resistive load Z_1 and the output power was 50.5 W, 2) the same inverter was loaded with an inductive load Z_2 and the apparent power was 51.4 VA, regarding these two conditions the modulation index A was set to 3.64, and 3) the resistive load Z_1 was changed with maintaining the output voltage at 50.0 V by adjusting the modulation index A from 3.53 to 3.64.

Fig. 13 shows observed waveforms with the resistive load Z_1 in the experiment. As shown in Fig. 13, the waveform of the bus voltage v_{bus} had nine steps, the output voltage was a clean sinusoidal waveform, and the capacitor voltages V_{C1} and V_{C2} were kept at twice the input voltage and capacitor voltage V_{C3} was kept at the same with the input voltage. These characteristics were well agreed with the simulation results. The measured value of the output voltage was 50.0 V and the power conversion efficiency was 96.0 %.

Fig. 14 shows the observed waveforms with the inductive load Z_2 in the experiment. From Fig. 14, there was no disturbance in the observed waveform, which were almost identical to the resistive load. As shown in Fig. 14(c), there was a phase difference between the output voltage and the output current. The measured power factor was 0.863 and the phase difference was 30.5 degrees. The measured value of the output voltage was 50.1 V and the power conversion efficiency was 96.4 %.

The spectra in the experiment are shown in Fig. 15. Fig. 15(a) and (b) are the spectra of the bus voltage v_{bus} and the output current i_{out} with the resistive load Z_1. Fig. 11(c) and (d) are their spectrums with the inductive load Z_2. Under the resistive load condition as shown in the Fig. 15(a) and (b), THD of the bus voltage and the output current were respectively 17.3% and 1.88%. Under the inductive load condition as shown in the Fig. 15(c) and (d), THD of the bus voltage and the output current were respectively 17.0% and 0.33%. From Fig. 15, it was also confirmed that the proposed inverter operates accurately even in inductive load.

According to [36], approximate voltage THD can be expressed as

$$THD = \frac{57.7}{(h-1)A}, \tag{15}$$

where h is non-negative level count (5 for a nine-level inverter). Therefore, the voltage THD at the modulation index of 3.64 (according to [36], this value equals 0.91) is estimated as 15.9%, which is well agreed with the experimental results.

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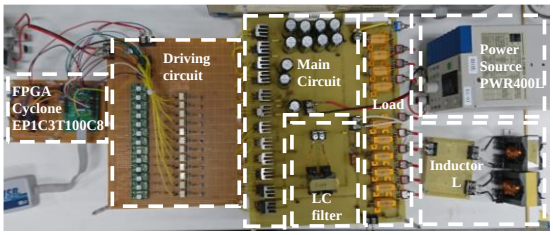
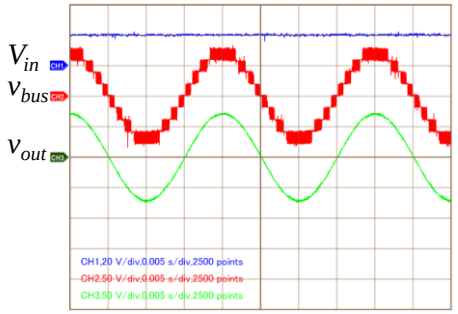
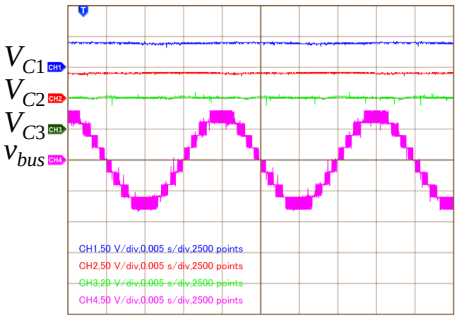


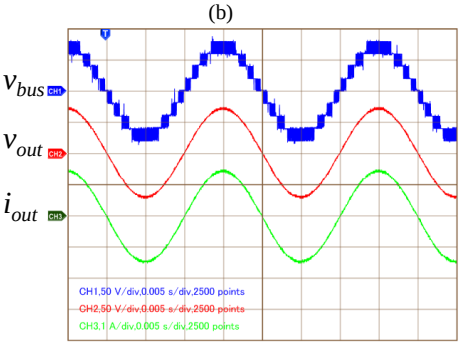
Fig. 12 A picture of the boost type nine level switched capacitor inverter.



(a)

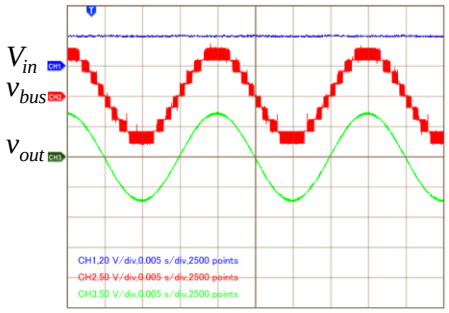


(b)

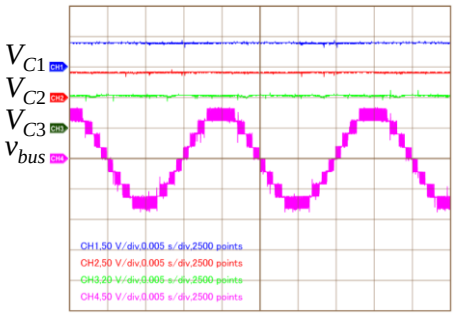


(c)

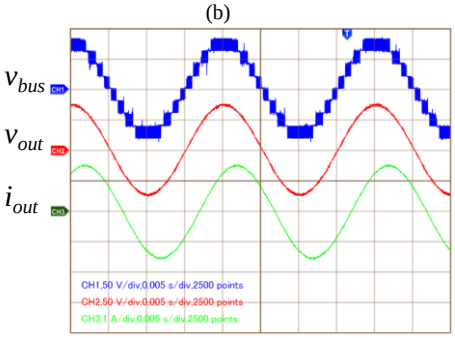
Fig. 13 Observed waveforms with the resistive load Z_1 in the experiment, (a) input voltage V_{in}, bus voltage v_{bus}, and output voltage v_{out}, (b) capacitor voltages V_{C1}-V_{C3} and bus voltage v_{bus}, (c) bus voltage v_{bus}, output voltage v_{out}, and output current i_{out}.



(a)



(b)



(c)

Fig. 14 Observed waveforms with the inductive load Z_2 in the experiment,(a) input voltage V_{in}, bus voltage v_{bus}, and output voltage v_{out}, (b) capacitor voltages V_{C1}-V_{C3} and bus voltage v_{bus}, ,(c) bus voltage v_{bus}, output voltage v_{out}, and output current i_{out}.

Fig. 16 shows power conversion efficiencies as functions of the output power P_{out}. The measured power conversion efficiency was maintained over 96.0% from 5.01 W to 50.5 W. The measured maximum power conversion efficiency was 97.3 %, when the output power was 20.2 W with 3.57 of modulation index. In the simulation, the maximum power conversion efficiency was 97.7 %, when the output power was 20.2 W with 3.57 of modulation index. The power conversion efficiency decreased as the output power increased, which could be caused by the increase of the capacitor voltage ripple. These characteristics were also confirmed in the simulation. The difference between the simulation and the experiment could be caused by the line impedance. Fig. 17 shows behavior of the proposed inverter under load variation. Even if the output power was changed from 5.01 W to 50.5 W, the bus voltage v_{bus} was not distorted, and the capacitor voltages were kept constant.

V. 2 kW Scaled Inverter Simulation

A 2kW scaled inverter was designed and simulated. Table V shows the parameters of the proposed inverter designed at 2kW. The on-resistances r_{DS1} - r_{DS7}, r_{DS10} and the drain-source capacitances C_{DS1} - C_{DS7}, C_{DS10} of the MOSFETs S_1 – S_7, S_{10} were determined based on the datasheet of IXFK170KN20T. The on resistances r_{DS8} and r_{DS9}, and the drain-source capacitances C_{DS8} and C_{DS9} of the MOSFETs S_8 and S_9 were based on the datasheet of IPB320N20N3. With respect to S_{11} and S_{12}, two cases were considered. One uses MOSFETs and the other uses IGBTs. In the case of MOSFETs, the parameters were determined based on the datasheet of FQA30N40, and the simulation model is shown in Fig. 8. On the other hand, in the case of IGBTs, the parameters were determined based on the datasheet of IRGB4620D.

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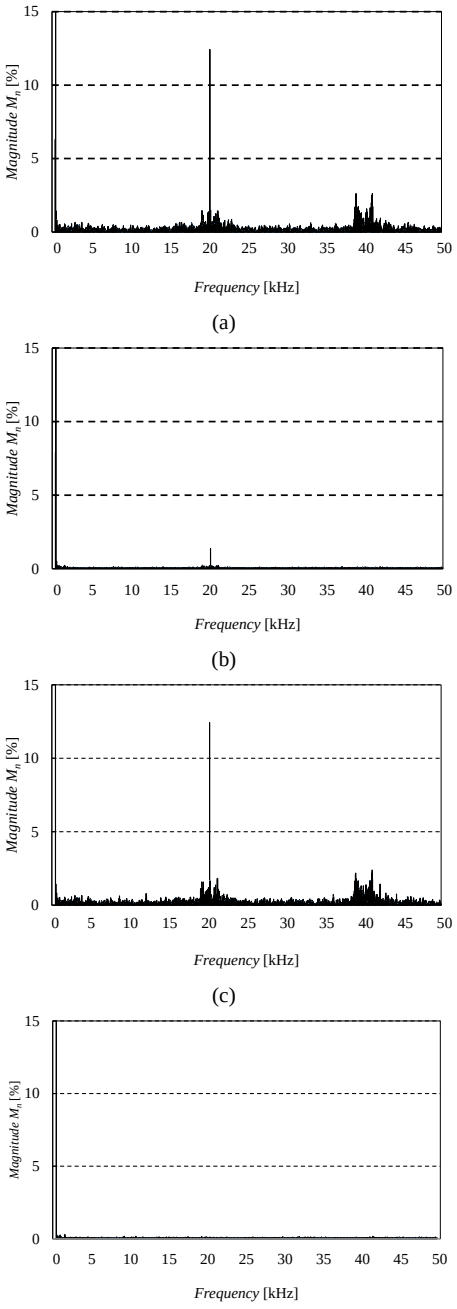

Fig. 15 The spectrums in the experiment, (a) bus voltage v_{bus} with the resistive load Z_1, (b) output current i_{out} with the resistive load Z_1, (c) bus voltage v_{bus} with the inductive load Z_2, (d) output current i_{out} with the inductive load Z_2.

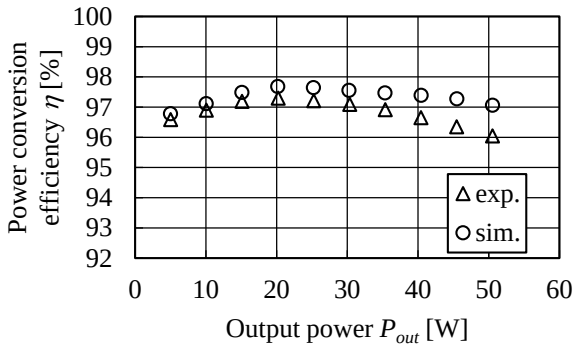

Fig. 16 Measured power conversion efficiency η as a function of the output power P_{out}.

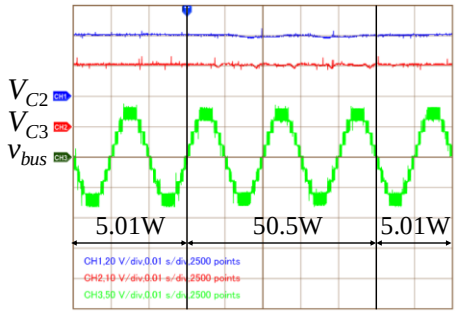

Fig. 17 Behavior of proposed inverter under load variation.

Table V Parameters of the proposed inverter designed for 2kW

Parameters	Value
Input voltage V_{in}	80.0 V(r_{in} : 50 mΩ)
Modulation index A	3.64
Output load R_o	R: 400 ~ 18.2 Ω
MOSFETs S_1 ~ S_7, S_{10}	r_{DS1} ~ r_{DS7}, r_{DS10} : 11.0 mΩ C_{DS1} ~ C_{DS7}, C_{DS10} : 1735 pF
MOSFETs S_8, S_9	r_{DS1} ~ r_{DS10} : 32.0 mΩ C_{DS1} ~ C_{DS10} : 131 pF
MOSFETs S_{11}, S_{12}	r_{DS11}, r_{DS12} : 140 mΩ C_{DS11}, C_{DS12} : 607 pF
IGBTs S_{11}, S_{12}	V_{on11}, V_{on12} : 1.55V C_{CE11}, C_{CE12} : 29.0 pF
Capacitor C_1, C_2	4.00 mF (r_{C1}, r_{C2} : 18.0 mΩ)
Capacitor C_3	2.00 mF (r_{C3} : 36.0 mΩ)
Capacitor C_S	1.00 mF (r_{CS} : 40.0 mΩ)
Filter inductor L_f	1.05 mH (r_{Lf} : 58.8 mΩ)
Filter Capacitor C_f	487 μF (r_{Cf} : 201 mΩ)
Switching frequency f_s	20.0 kHz
Frequency of the reference waveform f_{ref}	50.0 Hz
Time step	1.00×10^{-8} s

The simulation model in this case is shown in Fig. 18. Each capacitance was designed to have a voltage ripple less than 10% and ESR was determined based on the value obtained by measuring LKX2D222MESC50 with an impedance meter.

Fig. 19 shows observed waveforms at 2 kW using MOSFETs in the simulation. From Fig.19, each waveform was well agreed with the theory as in Section III. The THD of the bus voltage and the output current were 16.68 % and 1.85 %, respectively. Fig. 20 shows characteristics of power conversion efficiency η as functions of the output power P_{out}. The maximum power conversion efficiency was 97.6 % at the output power P_{out} = 0.411 kW using MOSFETs. The power conversion efficiency at 0.985 kW and 1.99 kW using MOSFETs were 96.1% and 92.2%, respectively. On the other hand, the power conversion efficiency at 0.978 kW and 199 kW using IGBTs were 95.1% and 91.9%, respectively. Under the condition of less than 2kW, it was not advantageous to use IGBTs. The THD of bus voltage and output voltage at 1.99 kW using MOSFETs were 16.9% and 1.85%, respectively.

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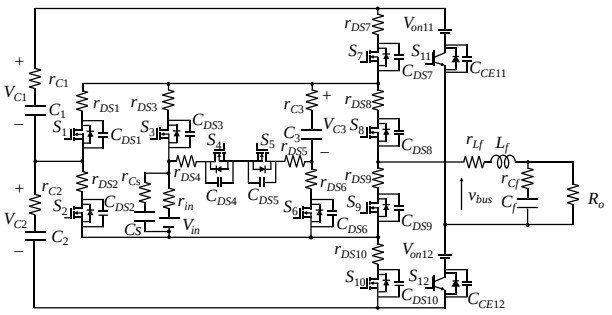
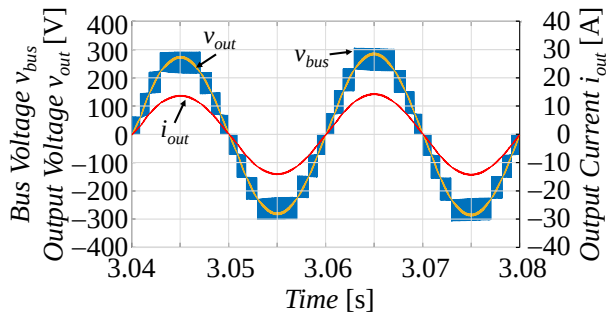
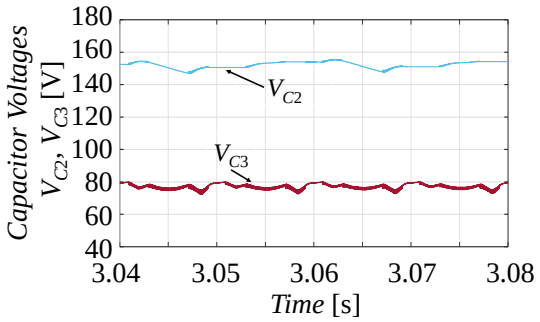


Fig. 18 Simulation model of proposed inverter (using IGBTs).



(a)



(b)

Fig. 19 Observed waveform at 2kW using MOSFETs, (a) bus voltage v_{bus}, output voltage v_{out}, output current i_{out}, (b) capacitor voltage V_{C2} and V_{C3}.

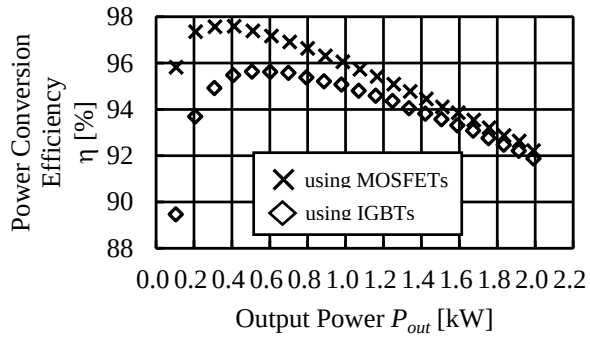


Fig. 20 Characteristics of power conversion efficiency η as a function of the output power P_{out}.

VI. Conclusion

A boost type nine-level switched capacitor inverter has been proposed. The operation principle, the modulation method, the voltage/current stress of switches, the determination of capacitances, the simulation results, and the experimental results were shown. The proposed inverter outputs nine-step voltage waveform with fewer components than conventional nine-level inverters. Furthermore, this inverter has a quadruple boost function owing to the switched capacitor structure. Therefore, no boost converter is required in the primary stage. The circuit operation has been confirmed with resistive load and with inductive load in both simulation and experiment. Those results were well agreed. Furthermore, power conversion efficiency was obtained when the output power changed from 5.01 W to 50.5 W under the fixed input voltage and the fixed output voltage. The measured maximum power conversion efficiency was 97.3 %, when the output power was 20.2 W with 3.57 of modulation index. In the simulation at 2 kW model, the power conversion efficiency at 0.985 kW and 1.99 kW were 96.1% and 92.2%, respectively.

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